IN THE CLAIMS

1. (Previously presented): A clock and data recovery circuit comprising:

- a first data input receiving a data signal of a first frequency;

- a clock defining a timing signal of a second frequency;

- a phase generator dividing a cycle of the timing signal into a number of N clock phases;

- a data sampling component sampling a portion of said data signal causing a logic output statement based on a truth table, said data sampling component comprising

- a buffer component for buffering said data signal, said buffer component triggered by a first clock phase i, a second clock phase j and a third clock phase k, resulting in a buffering of the state of said data signal at said clock phases i, j, and k and wherein the clock phases i, j, and k are interdependent by at least one of the equations:

$$j = i + N/2 - M \text{ and } k = i + N/2 \text{ if } i \leq N/2 \text{ and}$$

$$j = i - N/2 - M \text{ and } k = i - N/2 + M \text{ if } i > N/2$$

with a parameter M selectable within $0 < M < N/2$, and

- a phase detector coupled to said buffer component; and

- a phase selector coupled to said data sampling component.

2. (Previously presented) A clock and data recovery circuit as claimed in claim 1, further comprising:

a counter coupled between said data sampling component and said phase selector, wherein said logic output statement of said data sampling component causes said counter to count up, count down or hold.

3. (Original) A clock and data recovery circuit as claimed in claim 1, wherein

the data signal is a binary signal having signal states zero or one defining a bit sequence.

4. (Original) A clock and data recovery circuit as claimed in claim 1, wherein

said buffer component comprises bistable multivibrators.

5. (Previously presented) A clock and data recovery circuit as claimed in claim 1, wherein

said buffer component comprises a first, a second and a third buffer portion each having a data input and a data output, with the data inputs of the three buffer portions coupled to said first data input.

6. (Canceled).

7. (Canceled).

8. (Previously presented) A clock and data recovery circuit as claimed in claim 1, further comprising a first output receiving the data signal from the buffer portion which is triggered by the clock phase i,

wherein at least one of said data signal and said timing signal is transmitted by said first output.

9. (Previously presented) A clock and data recovery circuit as claimed in claim 5, wherein the signal states of the data signal at the data outputs of said first, second and third buffer portions are detected by said phase detector.

10. (Previously presented) A clock and data recovery circuit as claimed in claim 9, wherein

the phase detector further detects the signal state of the data signal at the clock phase ~~i~~ *i* of the previous cycle of the timing signal.

11. (Previously presented) A clock and data recovery circuit as claimed in claim 1, further comprising

a low pass filter coupled to said phase detector.

12. (Original) A clock and data recovery circuit as claimed in claim 1, further comprising

dual rail amplifiers.

13. (Currently amended) A method for clock and data recovery comprising the steps of:

- receiving a data signal of a first frequency;
- defining a timing signal of a second frequency;
- dividing a cycle of the timing signal into a number of *N* clock phases;

- sampling a portion of said data signal by a data sampling component resulting in a binary number, said data sampling component comprising a buffer component buffering said data signal and comprising a phase ~~detector;~~

~~looking~~ detector that looks up said binary number in a truth table yielding a logic output statement; and

- transmitting said logic output statement to a phase selector;

wherein the data signal is a binary signal having signal states zero or one defining a bit sequence and wherein said data signal is buffered by a first, a second and a third group of bistable multivibrators, triggered by a first clock phase *i*, a second clock phase *j* and a third clock phase *k*, respectively, resulting in a buffering of the state of said data signal at said clock phases *i*, *j*, and *k*.

14. (Previously presented) A method as claimed in claim 13, wherein said transmitting step comprises the steps of (a) incrementing, decrementing, or holding a counter value in response to said logic output statement of the truth table and (b) transferring the counter value to the phase selector.

15. (Canceled).

16. (Previously presented) A method for clock and data recovery comprising the steps of:

- receiving a data signal of a first frequency;

- defining a timing signal of a second frequency;

- dividing a cycle of the timing signal into a number of N clock phases;

- sampling a portion of said data signal by a data sampling component resulting in a binary number, said data sampling component comprising a buffer component buffering said data signal and comprising a phase detector;

- looking up said binary number in a truth table yielding a logic output statement; and

- transmitting said logic output statement to a phase selector;

wherein the data signal is a binary signal having signal states zero or one defining a bit sequence and wherein the buffer component is triggered by a first clock phase i, a second clock phase j and a third clock phase k, resulting in a buffering of the state of said data signal at said clock phases i, j, and k; and

wherein the clock phases j and k are further defined by at least one of the equations:

$j = i + N/2 - M$ and $k = i + N/2$ if $i \leq N/2$ and

$j = i - N/2 - M$ and $k = i - N/2 + M$ if $i > N/2$

with selecting a parameter M within $0 < M < N/2$.

17. (Previously presented) A method as claimed in claim 13 or 16, further comprising the step of

transmitting at least one of said data signal and said timing signal by an output with the transmission triggered by the clock phase i.

18. (Currently Amended) A method for clock and data recovery further comprising the steps of:

- receiving a data signal of a first frequency;

- defining a timing signal of a second frequency;

- dividing a cycle of the timing signal into a number of N clock phases;

- sampling a portion of said data signal by a data sampling component comprising a buffer component buffering said data signal and comprising a phase detector, said step of sampling further including detecting the state of the data signal at a clock phase *i* of the previous cycle of the timing signal, resulting in a four digit binary number having sixteen possible ~~values;~~

~~- looking~~ values, wherein said phase detector looks up said four digit binary number in a truth table yielding a logic output statement; and

- transmitting said logic output statement to a phase selector.

19. (Currently amended) A clock and data recovery circuit comprising:

- a first data input receiving a data signal of a first frequency;

- a clock defining a timing signal of a second frequency;

- a phase generator dividing a cycle of the timing signal into a number of *N* clock phases;

- a data sampling component sampling a portion of said data signal ~~causing a logic output statement based on a truth table~~, said data sampling component comprising a buffer component for buffering said data signal and comprising a phase detector, coupled to said buffer component,

wherein said phase detector produces a logic output statement based on a truth table, and

wherein the phase detector further detects the signal state of the data signal at a clock phase *i* of the previous cycle of the timing signal; and

- a phase selector coupled to said data sampling component.

20. (Previously presented) A clock and data recovery circuit as claimed in claim 19, further comprising:

a counter coupled between said data sampling component and said phase selector, wherein said logic output statement of said data sampling component causes said counter to count up, count down or hold.

21. (Previously presented) A clock and data recovery circuit as claimed in claim 19, wherein the data signal is a binary signal having signal states zero or one defining a bit sequence.

22. (Previously presented) A clock and data recovery circuit as claimed in claim 19, wherein

said buffer component comprises bistable multivibrators.

23. (Previously presented) A clock and data recovery circuit as claimed in claim 19, said buffer component comprising a first, a second and a third buffer portion each

having a data input and a data output, with the data inputs of the three buffer portions coupled to said first data input.

24. (Previously presented) A clock and data recovery circuit as claimed in claim 19, further comprising a first output receiving the data signal from the buffer portion which is triggered by the clock phase *i*,

wherein at least one of said data signal and said timing signal is transmitted by said first output.

25. (Previously presented) A clock and data recovery circuit as claimed in claim 23, wherein the signal states of the data signal at the data outputs of said first, second and third buffer portions are detected by said phase detector.

26. (Previously presented) A clock and data recovery circuit as claimed in claim 19, further comprising

a low pass filter coupled to said phase detector.

27. (Previously presented) A clock and data recovery circuit as claimed in claim 19, further comprising

dual rail amplifiers.

28. (Currently Amended) A clock and data recovery circuit comprising:

- a first data input receiving a data signal of a first frequency;

- a clock defining a timing signal of a second frequency;

- a phase generator dividing a cycle of the timing signal into a number of *N* clock phases;

- a data sampling component ~~causing a logic output statement based on a truth table, said data sampling component~~ comprising

a buffer component buffering said data signal and

a phase detector that produces a logic output statement based on a truth table; and

- a phase selector coupled to said data sampling component;

wherein said data signal is buffered by a first, a second and a third group of bistable multivibrators, triggered by a first clock phase *i*, a second clock phase *j*, and a third clock phase *k*, respectively, resulting in a buffering of the state of said data signal at said clock phases *i*, *j*, and *k*.